UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,012	08/01/2003	Hong Wang	42P15447	4733

8791 7590 11/28/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TECKLU, ISAAC TUKU	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,012	WANG ET AL.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3/ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/01/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on 08/01/2003.

2. Claims 1-33 have been examined.

Oath/Declaration

3. The office acknowledges receipt of a properly signed oath/declaration filed on 08/01/2003.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the execution pipeline" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-3 and 6-7 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a" useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. §

101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

Specifically, claim 1 recites an apparatus including logic. From the specifications, nowhere is there any description as to whether a hardware embodiment is supporting the logic. Accordingly, software implemented components (provided with some functionality) claimed without a tangible storage in a computer medium so as to reasonably convey that when executed would yield computer data transformation leading to some concrete, and tangible result, amount to mere abstract ideas because such lack of hardware support would not enable the realization of such functionality into real-world results. As a whole, the apparatus claim is therefore rejected for leading to non-statutory subject matter for failing to the Practical Test application requirement as set forth above.

Claims 2-3, 6-7 are equally rejected for not remedying to the deficiency of the base claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Liao et al. (US 2004/0054990 A1).

Per claim 1, Liao discloses an apparatus comprising:

marking logic to mark instruction information for an instruction of a speculative thread as speculative (paragraph [0034] "... prefetch is executed in the speculative ...place the desired data in the cache ...");

blocker logic to prevent data associated with a store instruction of the speculative thread from being forwarded to an instruction of a non-speculative thread (paragraph [0043] "... out-of-context instructions are not included ..."), the blocker logic further to prevent the data from being stored in a memory system (..." paragraph [0045] "... ensures that no store instruction ..." and paragraph [0045] "... exclusion of store instructions ...").

Per claim 2, Liao discloses the apparatus of claim 1, wherein: blocker logic is further to allow the data associated with a store instruction of the speculative thread to be forwarded to an instruction of a second speculative thread (paragraph [0031] "... thread capable of speculatively prefetching the load data ..." and e.g. FIG. 6, element 614 and related text).

Per claim 3, Liao discloses the apparatus of claim 1, further comprising: a plurality of store request buffers (paragraph [0063] "... provides for copying of live-in values to a buffer ..." e.g. FIG. 7, element 714 and related text), each store request buffer including a speculation identifier field (paragraph [0063] "... speculative thread seeking access ..." e.g. FIG. 6, element 608 and related text).

Per claim 4, Liao discloses the apparatus of claim 1, wherein the memory system further comprises: a data cache that includes a safe-store indicator field associated with each entry of a tag array (paragraph [0023] "... desired data in the cache ...").

Per claim 5, Liao discloses the apparatus of claim 1, wherein: the blocker logic is included within the memory system (e.g. FIG. 12, element 1202 and related text).

Per claim 6, Liao discloses the apparatus of claim 1, wherein blocker logic further includes:

dependence blocker logic to prevent data associated with a speculative store instruction from being forwarded to an instruction of the non-speculative thread (paragraph [0043] "... out-of-context instructions are not included ..." and paragraph [0045] "... ensures that no store instruction ..."); and

store blocker logic to prevent the data from being stored in a memory system (e.g. FIG. 6, element 614 and related text).

Per claim 7, Liao discloses the apparatus of claim 6, wherein: store blocker logic is outside the execution pipeline (e.g. FIG. 12, element 1202 and related text).

Per claim 8, Liao discloses the apparatus of claim 7, wherein: store blocker logic is included in the memory system.

Per claim 9, Liao discloses the apparatus of claim 6, wherein: dependence blocker logic is included in an execution pipeline (e.g. FIG. 12, element 1224 and related text).

Per claim 10, Liao discloses the apparatus of claim 9, wherein: dependence blocker logic is included in a memory ordering buffer (e.g. FIG. 12, element 1202 and related text).

Per claim 11, Liao discloses a system, comprising: a memory system that includes a dynamic random access memory; a processor including dependence blocker logic to prevent data associated with a store instruction of a speculative thread from being forwarded to an instruction of a non-speculative thread (e.g. FIG. 12 and related text); the processor further including store blocker logic to prevent the data from being stored in the memory system (paragraph [0045] "... exclusion of store instructions temporarily ...").

Per claim 12, Liao discloses the system of claim 11, wherein: the processor further includes marking logic to mark instruction information associated with the store instruction as speculative (paragraph [0034] "... prefetch is executed in the speculative ... place the desired data in the cache ..." and paragraph [0066] "... provide for speculative thread to spawn another speculative thread ...").

Per claim 13, Liao discloses the system of claim 12, wherein: the marking logic is further to associate a safe speculation domain ID with the instruction information (paragraph [0066] "... identification of spawn points ...").

Per claim 14, Liao discloses the system of claim 13, wherein: the marking logic is further to indicate a thread identifier as the speculation domain ID (paragraph [0066] "... provide for speculative thread to spawn another speculative thread ...").

Per claim 15, Liao discloses the system of claim 12, further comprising: a store request buffer to store the speculation domain ID (e.g. FIG. 12, element 1202 and related text).

Per claim 16, Liao discloses the system of claim 11, wherein: the processor includes a first logical processor to execute the non-speculative thread; and the processor includes a second logical processor to execute the speculative thread (e.g. FIG. 11 and related text).

Per claim 17, Liao discloses the system of claim 11, further comprising: a second processor that includes said dependence blocker logic and said store blocker logic; wherein said processor is to execute the non-speculative thread and said second processor is to execute the speculative thread (e.g. FIG. 11 and related text).

Per claim 18, Liao discloses the system of claim of claim 11, wherein: the memory system includes a cache organized to include a plurality of tag lines, wherein each tag line of the cache includes a unique helper thread ID field (paragraph [0023] "... desired data in the cache ...").

Per claim 19, Liao discloses the system of claim 11, wherein: the memory system includes a cache organized to include a plurality of tag lines, wherein each tag line of the cache includes a safe-store indicator field (paragraph [0034] "... prefetch is executed in the speculative ... place the desired data in the cache ..." and paragraph [0066] "... provide for speculative thread to spawn another speculative thread ...").

Per claim 20, Liao discloses the system of claim 11, wherein: the memory system includes a victim tag cache to indicate evicted cache lines that include speculative load data (e.g. FIG. 10 and related text).

Per claim 21, Liao discloses a method, comprising:

receiving instruction information for a load instruction, the instruction information including a load address (paragraph [0023] "...by a load instruction ...");

performing a dependence check, wherein performing the dependence check includes (e.g. FIG. 6, elements 606 and 608 and related text):

determining if a store address of an in-flight store instruction matches the load address (paragraph [0045] "... no store instructions ..."); and

determining if the load instruction and the in-flight store instruction each originate with a speculative thread; forwarding, if the dependence check is successful, store data associated with the in-flight store instruction to the load instruction (e.g. FIG. 6, element 606 and related text); and

declining to forward, if the dependence check is not successful, the store data to the load instruction (paragraph [0045] "... exclusion of store instructions ...").

Per claim 22, Liao discloses the method of claim 21, wherein performing the dependence check further comprises: determining if the in-flight store instruction and the load instruction originate from the same thread (e.g. FIG. 6, elements 606 and 608 and related text).

Per claim 23, Liao discloses the method of claim 22, wherein determining if the in-flight store instruction and the load instruction originate from the same thread further comprises: determining if a thread ID associated with the in-flight store instruction matches a thread ID associated with the load instruction (paragraph [0023] "... desired data in the cache ...").

Per claim 24, Liao discloses the method of claim 21, wherein performing the dependence check further comprises: if the load instruction and the in-flight store instruction do not each originate with a speculative thread, determining if the load instruction and the in-flight store instruction each originate with a non-speculative thread (e.g. FIG. 6, elements 606 and 608 and related text).

Per claim 25, Liao discloses the method of claim 21, further wherein: declining to forward further comprises declining to forward the store data to the load instruction if (the load instruction and the in-flight store instruction each originate with a speculative thread) and (the in-flight store instruction originates with a speculative thread that is not older in program order than the speculative thread from which the load instruction originates) (e.g. FIG. 6, elements 606 and 608 and related text).

Per claim 26, Liao discloses a method, comprising: processing a speculative thread cache read request; processing a speculative thread cache write request; and processing a cache access request from a non-speculative thread (paragraph [0023] "... higher-level cache ...").

Per claim 27, Liao discloses the method of claim 26, wherein processing a speculative thread cache read request further comprises: forwarding speculative data from a cache to a speculative thread responsive to a data cache read request (paragraph [0043] "... out-of-context instructions are not included ..." and paragraph [0045] "... ensures that no store instruction ...").

Per claim 28, Liao discloses the method of claim 26, wherein processing a speculative thread cache read request further comprises: forwarding non-speculative store data from a cache to a speculative thread responsive to a data cache read request (paragraph [0043] "... out-of-context instructions are not included ..." and paragraph [0045] "... ensures that no store instruction ...").

Per claim 29, Liao discloses the method of claim 26, wherein processing a cache access request from a non-speculative thread further comprises: forwarding non-speculative data from a cache to a non-speculative thread responsive to a data cache read request (e.g. FIG. 10 and related text).

Per claim 30, Liao discloses the method of claim 26, wherein processing a cache access request from a non-speculative thread further comprises: if a cache does not include a cache line

associated with the cache access request, allocating a new cache line (paragraph [0023] "... prevent cache miss ...");

wherein allocating a new cache line further comprises: if the new cache line includes dirty speculative data, allocating the new cache line without generating a writeback operation; and if the new cache line includes dirty non-speculative data, generating a writeback operation (paragaraph [0023] "... allow the helper thread to execute in time ...").

Per claim 31, Liao discloses the method of claim 26, wherein processing a speculative thread cache write request further comprises: allowing the speculative thread to write data to the cache if a cache line corresponding to the cache write request includes speculative data (paragaraph [0023] "... allow the helper thread to execute in time ...").

Per claim 32, Liao discloses the method of claim 26, wherein processing a speculative thread cache write request further comprises: if the cache line corresponding to the cache write request contains dirty non-speculative data in the cache line corresponding to the data cache request: generating a writeback of the dirty non-speculative data; allowing the speculative thread to write speculative data to the cache line (paragaraph [0023] "... allow the helper thread to execute in time ..."); and marking the cache line as speculative (paragraph [0034] "... prefetch is executed in the speculative ... place the desired data in the cache ...").

Per claim 33, Liao discloses the method of claim 26, wherein processing a speculative thread cache write request further comprises: if the cache does not contain data in a cache line corresponding to the data cache address: allocating a new cache line (paragraph [0023] "... prevent cache miss ..."); marking the new cache line as speculative (paragraph [0034] "... prefetch is executed in the speculative ... place the desired data in the cache ..."); and allowing the speculative thread to write speculative data to the new cache line (paragaraph [0023] "... allow the helper thread to execute in time ...").

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Isaac Tecklu
Art Unit 2192

TUAN DAM
SUPERVISORY PATENT EXAMINER